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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/618,704 | 07/15/2003 | Keisuke Kanamaru | 8009-1014 | 4914 |

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| EXAMINER | |
|---|---|
| LEVIN, NAUM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-13

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/618,704 | KANAMARU ET AL. | |
| | Examiner | Art Unit | |
| | Naum B. Levin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being unpatentable by Banik (US Patent 6,185,720).

As to claims 1, 6 and 11 Banik discloses:

(1) A delay optimization designing system for a logic circuit including a plurality of flip-flops and a combinational circuit formed from logic circuit elements, comprising (col.1, ll.49-54; col.4, ll.7-14):

flip-flop selection means (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for selecting any flip-flop not to be substituted (replaced) into a latch from within a given logic circuit (col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43);

flip-flop searching means (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for searching any flip-flop having a delay margin from among the flip-flops which are not selected (not selected to

be replaced by latch) by said flip-flop selection means (col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43); and

latch substitution means (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for substituting any flip-flop searched by said flip-flop searching means into latch which passes a signal to the output side therethrough faster than the searched flip-flop (removing a slave latch of a master/slave flip-flop from the data path if the propagation delay of the data path is longer than the particular time duration and route output data from a master latch of the master/slave flip-flop to a pulse latch) (col.4, ll.32-44; col.6, ll.6-9; col.6, ll.45-59; col.7, ll.38-43);

(6) A delay optimization designing method for a logic circuit including a plurality of flip-flops and a combinational circuit formed from logic circuit elements, comprising (col.1, ll.49-54; col.4, ll.7-14):

flip-flop selection step (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for selecting any flip-flop not to be substituted (replaced) into a latch from within a given logic circuit (col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43);

flip-flop searching step (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for searching any flip-flop

having a delay margin from among the flip-flops which are not selected (not selected to be replaced by latch) by said flip-flop selection means (col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43); and

latch substitution step (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for substituting any flip-flop searched by said flip-flop searching means into latch which passes a signal to the output side therethrough faster than the searched flip-flop (removing a slave latch of a master/slave flip-flop from the data path if the propagation delay of the data path is longer than the particular time duration and route output data from a master latch of the master/slave flip-flop to a pulse latch) (col.4, ll.32-44; col.6, ll.6-9; col.6, ll.45-59; col.7, ll.38-43);

(11) A delay optimization designing program for causing a computer to perform a delay optimization designing method for a logic circuit including a plurality of flip-flops and a combinational circuit formed from logic circuit elements, comprising (col.1, ll.49-54; col.4, ll.7-14; col.8, ll.12-15):

flip-flop selection step (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for selecting any flip-flop not to be substituted (replaced) into a latch from within a given logic circuit (col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43);

flip-flop searching step (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for searching any flip-flop having a delay margin from among the flip-flops which are not selected (not selected to be replaced by latch) by said flip-flop selection means (col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43); and

latch substitution step (processor/steps can be carried out by any of a wide variety of conventional circuit design and/or emulation machines or systems, either hardwired or operating under software control, col.5, ll.60-63) for substituting any flip-flop searched by said flip-flop searching means into latch which passes a signal to the output side therethrough faster than the searched flip-flop (removing a slave latch of a master/slave flip-flop from the data path if the propagation delay of the data path is longer than the particular time duration and route output data from a master latch of the master/slave flip-flop to a pulse latch) (col.4, ll.32-44; col.6, ll.6-9; col.6, ll.45-59; col.7, ll.38-43).

As to claims 2-5, 7-10 and 12-15 Banik discloses:

(2), (7), (12) A delay optimization designing system/method/program for a logic circuit, wherein the flip-flop holds data inputted response to an edge of clock upon variation from a first level a second level, and the latch substituted by said latch substitution means passes input data when the clock indicates the first level therethrough to the output side (col.2, ll.41-67; col.3, ll.1-15);

(3-5), (8-10), (13-15) A delay optimization designing system/method/program for a logic circuit, further comprising latch insertion means for inserting a second latch, which passes input data at a timing different from that the latch substituted by said latch substitution means, into predetermined portion of the logic circuit (col.5, ll.4-14; col.5, ll.58-67; col.6, ll.1-5; col.6, ll.10-13; col.6, ll.45-59; col.7, ll.34-43).

## *Conclusion*

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kudlugi et al. (US Patent 6,817,001) recites emulation of logic and memory circuits. The gate signal of a latch is scheduled to arrive prior to the data signal of the latch. The output value of the latch is evaluated after the arrival of the data signal. Emulation of flip-flops can be achieved by replacing each flip-flop by a master slave latch pair to satisfy hold time requirement at each latch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AU-2825